CLAIMS

1. (original) A circuit for improving signal integrity in a memory system comprising:
a transmission line comprising a dampening impedance between a driver and a branch point of said transmission line; and

a termination impedance having one end coupled to said transmission line between said dampening impedance and said branch point;

said transmission line having branches from said branch point and coupled to memory module interfaces, said branches having respective lengths between said branch point and said memory module interfaces to be configured symmetrically, wherein said branch point is at a point to balance signal transmission on said branches.

2. (original) The circuit of Claim 1, wherein said transmission line is bi-directional.

3. (original) The circuit of Claim 1, wherein two of said branches have substantially the same length.

4. (original) The circuit of Claim 3, wherein a third of said branches does not have substantially the same length as said two of said branches.

5. (original) The circuit of Claim 1, wherein said circuit provides signal integrity for memory modules having a double high configuration.

6. (original) The circuit of Claim 1, wherein said branches couple to an odd number of memory module interfaces and wherein at least one pair of branches have substantially the same length.

7. (original) The circuit of Claim 1, wherein said branches couple to an even number of memory module interfaces and wherein pairs of branches have substantially the same length.

8. (original) The circuit of Claim 1, wherein said termination impedance is connected to said dampening impedance.

9. (original) The circuit of Claim 1, further comprising a receiver coupled to said transmission line, wherein said dampening impedance is between said receiver and said branch point.

10. (original) A circuit for improving signal integrity in a memory system comprising:

a plurality of memory modules;

a data line having a first end and a second end, said data line coupling said memory modules; and

a transmission line having a series resistance and a parallel resistance in a stub configuration;

said transmission line having a first end coupled to a driver and a second end connected at a point on said data line to balance signal transmission between said point on said data line and said first and second ends of said data line.

11. (original) The circuit of Claim 10, wherein said transmission line is bi-directional.

12. (original) The circuit of Claim 10, wherein said transmission line is connected at substantially the midpoint of said data line.

13. (original) The circuit of Claim 10, wherein said termination impedance is connected to said dampening impedance.

14. (original) The circuit of Claim 10, further comprising a receiver coupled to said first end of said transmission line.

15. (original) The circuit of Claim 10, wherein said plurality of memory have a double high configuration.

16. (original) The circuit of Claim 10, wherein said plurality of memory modules is an odd number and wherein said second end of said transmission line is connected to said data line at the middle memory module.

17. (original) The circuit of Claim 10, wherein said plurality of memory modules is an even number and wherein said second end of said transmission line is connected to said data line at a point substantially midway between two memory modules closest to the mid-point of said data line.

18. (original) A system comprising:

a bus controller;

a transmission line comprising a series impedance between a driver and a branch point of said transmission line; and

a parallel impedance having a first end coupled to said transmission line between said dampening impedance and said branch point and a second end coupled to a termination voltage terminal;

said transmission line having branches coupled to memory module interfaces, said branches having respective lengths between said branch point and said memory module interfaces to be configured symmetrically, wherein said branch point is at a point to balance signal transmission on said branches.

19. (original) The system of Claim 18, wherein said transmission line is bi-directional.

20. (original) The system of Claim 18, wherein two of said branches have substantially the same length.

21. (original) The system of Claim 20, wherein a third of said branches does not have substantially the same length as said two of said branches.

22. (original) The system of Claim 18, wherein said circuit provides signal integrity for memory modules having a double high configuration.

23. (original) The system of Claim 18, wherein said branches couple to an odd number of memory modules and wherein at least one pair of branches have substantially the same length.

24. (original) The system of Claim 18, wherein said branches couple to an even number of memory modules and wherein pairs of branches have substantially the same length.

25. (original) The system of Claim 18, further comprising a receiver coupled to said transmission line, wherein said dampening impedance is between said receiver and said branch point.